CLAIMS

We claim:

1. A method of forming a low-k dielectric material layer, comprising the steps of:

forming a first dielectric material sub-layer over a substrate;

treating the first dielectric material sub-layer with an energy treatment to form a hardened layer on the upper surface of the first dielectric material sub-layer; and

forming a second dielectric material sub-layer over the hardened layer; wherein the first dielectric sub-layer, the hardened layer and the second dielectric sub-layer comprise the low-k dielectric material layer.

2. The method of claim 1, wherein the first dielectric material sub-layer is comprised of SiOC.

3. The method of claim 1, wherein the first dielectric material sub-layer has a dielectric constant of from about 2.3 to 2.6.

4. The method of claim 1, wherein the first dielectric material sub-layer has a dielectric constant of greater than about 2.8.

5. The method of claim 1, wherein the hardened layer has a thickness of from about 250 to 500Å.

6. The method of claim 1, wherein the hardened layers has a thickness of from about 300 to 450Å.

7. The method of claim 1, wherein the energy treatment is conducted in situ.

8. The method of claim 1, wherein the energy treatment is conducted ex situ.

9. The method of claim 1, wherein the energy treatment is conducted using H_2.

10. The method of claim 1, wherein the energy treatment is conducted under the following conditions:

H_2 flow: from about 1600 to 2400 sccm;

temperature: from about 300 to 450°C;

pressure: from about 4.5 to 9.0mTorr;

time: from about 30 to 240 seconds; and

power: from about 300 to 1500 W.

11. The method of claim 1, wherein the energy treatment is conducted under the following conditions:

H_2 flow: from about 1800 to 2200 sccm;

temperature: from about 350 to 400°C;

pressure: from about 6.0 to 7.5 mTorr;

time: from about 90 to 180 seconds; and

power: from about 600 to 1200 W.

12. The method of claim of claim 1, wherein the hardened layer is an etch stop layer.

13. The method of claim 1, including the steps of:

patterning the second dielectric material sub-layer, the hardened layer and the first dielectric material sub-layer to form a via opening exposing a portion of the substrate ; and

then, using the hardened layer as an etch stop layer, patterning the second dielectric material sub-layer to form a trench opening over the via opening and exposing portions of the hardened layer.

14. The method of claim 1, including the steps of:

patterning the second dielectric material sub-layer, the hardened layer and the first dielectric material sub-layer to form a via opening exposing a portion of the substrate ; and

then, using the hardened layer as an etch stop layer, patterning the second dielectric material sub-layer to form a trench opening over the via opening and exposing portions of the hardened layer;

the trench opening and the via opening comprising a dual damascene opening.

15. The method of claim 1, including the steps of:

patterning the second dielectric material sub-layer, the hardened layer and the first dielectric material sub-layer using an overlying first patterned mask layer to form a via opening exposing a portion of the substrate ; and

then, using the hardened layer as an etch stop layer, patterning the second dielectric material sub-layer using an overlying second patterned mask layer to form a trench opening over the via opening and exposing portions of the hardened layer.

16. A method of forming a dielectric material layer, comprising the steps of:

sequentially forming one or more dielectric material sub-layers over a structure;

treating each sequentially formed one or more dielectric material sub-layers in sequence with a respective hydrogen treatment to form respective hard layers on the upper surface of each respective sequentially formed one or more dielectric material sub-layers; and

forming an uppermost dielectric material sub-layer over the sequentially formed one or more dielectric material sub-layers and respective hard layers to complete formation of the dielectric material layer.

17. The method of claim 16, wherein the sequentially formed one or more dielectric material sub-layers are each comprised of SiOC.

18. The method of claim 16, wherein the sequentially formed one or more dielectric material sub-layers each have a dielectric constant of from about 2.3 to 2.6.

19. The method of claim 16, wherein the sequentially formed one or more dielectric material sub-layers each have a dielectric constant of greater than about 2.8.

20. The method of claim 16, wherein each of the respective hard layers has a thickness of from about 250 to 500Å.

21. The method of claim 16, wherein each of the respective hard layers has a thickness of from about 300 to 450Å.

22. The method of claim 16, wherein the one or more respective hydrogen treatments are conducted in situ.

23. The method of claim 16, wherein the one or more respective hydrogen treatments are conducted ex situ.

24. The method of claim 16, wherein the one or more respective hydrogen treatments are conducted using H_2.

25. The method of claim 16, wherein the one or more respective hydrogen treatments are conducted under the following conditions:

H_2 flow: from about 1600 to 2400 sccm;

temperature: from about 300 to 450°C;

pressure: from about 4.5 to 9.0mTorr;

time: from about 30 to 240 seconds; and

power: from about 300 to 1500 W.

26. The method of claim 16, wherein the one or more respective hydrogen treatments are conducted under the following conditions:

H_2 flow: from about 1800 to 2200 sccm;

temperature: from about 350 to 400°C;

pressure: from about 6.0 to 7.5 mTorr;

time: from about 90 to 180 seconds; and

power: from about 600 to 1200 W.

27. The method of claim of claim 16, wherein the one or more of the respective hard layers are etch stop layers.

28. The method of claim 16, wherein there is one dielectric material sub-layer having a hard layer formed thereover by the respective hydrogen treatment.

29. The method of claim 16, wherein there is one dielectric material sub-layer having a hard layer formed thereover by the respective hydrogen treatment; and including the steps of:

patterning the uppermost dielectric material sub-layer, the hard layer and the one dielectric material sub-layer to form a via opening exposing a portion of the structure; and

then, using the hard layer as an etch stop layer, patterning the uppermost dielectric material sub-layer to form a trench opening over the via opening and exposing portions of the hard layer.

30. The method of claim 16, wherein there is one dielectric material sub-layer having a hard layer formed thereover by the respective hydrogen treatment; and including the steps of:

patterning the uppermost dielectric material sub-layer, the hard layer and the one dielectric material sub-layer to form a via opening exposing a portion of the structure; and

then, using the hard layer as an etch stop layer, patterning the uppermost dielectric material sub-layer to form a trench opening over the via opening and exposing portions of the hard layer;

the trench opening and the via opening comprising a dual damascene opening.

31. The method of claim 16, wherein there is one dielectric material sub-layer having a hard layer formed thereover by the respective hydrogen treatment; and including the steps of:

patterning the uppermost dielectric material sub-layer, the hard layer and the one dielectric material sub-layer using an overlying first patterned mask layer to form a via opening exposing a portion of the structure; and

then, using the hard layer as an etch stop layer, patterning the uppermost dielectric material sub-layer using an overlying second patterned mask layer 30 to

form a trench opening over the via opening and exposing portions of the hard layer.

32. A dual damascene structure, comprising:

a substrate;

a first patterned dielectric material sub-layer over the substrate;

a patterned hardened sub-layer upon the first patterned dielectric material sub-layer; the patterned hardened sub-layer and the first patterned dielectric material sub-layer having a via opening therethrough exposing a portion of the substrate; and

a second patterned dielectric material sub-layer upon the patterned hardened sub-layer; the second patterned sub-layer having a trench opening therethrough over the via opening.

33. The structure of claim 32, wherein the first and second patterned dielectric material sub-layers are each comprised of SiOC.

34. The structure of claim 32, wherein the first and second patterned dielectric material sub-layers each have a dielectric constant of from about 2.3 to 2.6.

35. The structure of claim 32, wherein the first and second patterned dielectric material sub-layers each have a dielectric constant of greater than about 2.8.

36. The structure of claim 32, wherein the hardened layer has a thickness of from about 250 to 500Å.

37. The structure of claim 32, wherein the hardened layer has a thickness of from about 300 to 450Å.

38. The structure of claim 32, wherein the hardened layer is an etch stop layer.

39. A dielectric material structure, comprising:

a substrate;

one or more dielectric material sub-layers over the substrate;

one or more respective hardened layers upon the one or more dielectric material sub-layers; and

an uppermost dielectric material sub-layer upon the uppermost one or more respective hardened layer.

40. The structure of claim 39, wherein the one or more dielectric material sub-layers and the uppermost dielectric material sub-layer are each comprised of SiOC.

41. The structure of claim 39, wherein the one or more dielectric material sub-layers and the uppermost dielectric material sub-layer each have a dielectric constant of from about 2.3 to 2.6.

42. The structure of claim 39, wherein the one or more dielectric material sub-layers and the uppermost dielectric material sub-layer each have a dielectric constant of greater than about 2.8.

43. The structure of claim 39, wherein the one or more respective hardened layers each have a thickness of from about 250 to 500Å.

44. The structure of claim 39, wherein the one or more respective hardened layers each have a thickness of from about 300 to 450Å.

45. The structure of claim 39, wherein the one or more respective hardened layers are etch stop layers.